Total No. of Questions : 8] **[Total No. of Pages : 2**

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[4065] - 625

M.E. (E & T/C) (VLSI & Embedded Systems)

ANALOG AND DIGITAL CMOS IC DESIGN

(2008 Course) (504181) (Sem. - I)

Time : 3 Hours] ***[Max. Marks : 100***

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answer to the two sections should be written in separate answer books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) What is body effect in case of MOSFET? What is latch-up problem in CMOS? How to overcome it? **[4]**

b) What is MOS model? What are its objectives? How it is used by designers? **[4]**

c) Where and How MOSFET is used as diode/Active Resistor? **[8]**

Q2) a) Use self-biased high-swing cascode current sink configuration to design a current sink of 250 μA and a V_{MIN} of 0.5V. Assume suitable data. **[8]**

b) Explain in detail the concept of BGR with its necessity. **[8]**

Q3) a) Current mirrors are based on which principle? Explain in short non-ideal effects of current mirrors. What is the use of current mirrors? **[8]**

b) Explain various architectures of High gain amplifier. **[8]**

Q4) Write short notes on any three : **[18]**

a) Active Load Inverter & its parameters.

b) Techniques used in Micro power opamp.

c) Current Amplifiers.

d) Buffered Op Amps using MOSFETs.

P.T.O.

SECTION - II

Q5) a) In CMOS technology why do we design the size of pMOS to be higher than the nMOS? Why PMOS and NMOS are sized equally in a transmission gate? **[4]**

b) Why is NAND gate preferred over NOR gate for implementing a design using CMOS logic? Design NAND gate using pass transistor logic and transmission gate. **[4]**

c) Consider a complex CMOS logic gate that implements the function **F = (A.B + C.D.E)'** **[8]**

i) Design the circuit.

ii) An inverter with $\beta n = \beta p$ is used as a sizing reference. Find the device sizes in the gate if we chose to equalize the nMOS and pMOS resistances.

Q6) a) What is metastability? How long does it stay in this state? What are the cases in which metastability occurs? How do designer tolerate metastability? **[8]**

b) Compare Domino and NORA high performance CMOS logic circuits. Explain NORA CMOS logic in detail. **[8]**

Q7) Design FSM controller for a coin - operated vending machine. Machine dispenses candy under the following conditions: **[16]**

- The machine accepts 1 rupee and 2 rupee coins. Only one coin at particular instant.
- It takes 3 rupees for a piece of candy to be released from the machine.
- If 4 rupees are deposited, the machine will not return the change, but it will credit the buyer with 1 rupee and wait for the buyer to make a second purchase.

Draw the minimized state diagram. Write VHDL code and test bench for the same.

Q8) Write short notes on any three : **[18]**

a) Significance and Types of Hazards.

b) Technology Scaling: Types and effects.

c) CMOS Parasitic.

d) Power dissipations and PDP in CMOS logic.

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