Total No. of Questions : 8] **[Total No. of Pages : 2**

P1650 **[3665] - 127 - A**

M.E. (E & T/C.) VLSI & Embedded Systems

ANALOG AND DIGITAL CMOS IC DESIGN

Time : 3 Hours] ***[Max. Marks : 100***

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Calculate W/L for MOSFET to offer dynamic resistance of 10 kΩ. Assume suitable data. **[8]**

b) With the help of necessary schematic explain current sink & source with Rout offered. **[8]**

Q2) Design CMOS differential amplifier for CMRR = 40dB. The dissipation should not exceed 2.5 mW at supply of 2.5V. **[16]**

Q3) a) What is design technique for low noise opamp? Brief with the help of necessary expressions. **[8]**

b) What is meant by buffered opamp? Explore with schematic. **[8]**

Q4) Write short notes on any three : **[18]**

a) Cascode amplifier.

b) Current mirrors.

c) Bandgap reference.

d) Micro power opamp.

SECTION - II

Q5) Draw FSM diagram & write VHDL code for 001101 Moor sequence detector. Also write test bench for it. **[16]**

P.T.O.

Q6) a) Explore CMOS parasitics in detail. How do they affect performance? **[8]**

b) What is need of NORA logic? With suitable schematic explore the typical logic function. **[8]**

Q7) a) What are the advance trends in high speed VLSI? **[8]**

b) For CMOS logic derive the expressions for total power dissipation & PDP. **[8]**

Q8) Write short notes on any three : **[18]**

a) Merits & demerits of transmission gate.

b) Technology scaling & its effects.

c) Hazards & mitigation techniques.

d) Low power design.