Total No. of Questions :8]

SEAT No :

P4509

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M.E. (E & T/C) (VLSI & Embedded Systems)

ANALOG AND DIGITAL CMOS IC DESIGN

(2008 Course) (504181) (Semester - I)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Use different answer sheet for each section.***
2) ***Attempt any 3 Questions from each section.***
3) ***Figures to the right indicate full marks.***

SECTION - I

Q1) a) What are the performance parameters of voltage reference circuit? Explore in brief. What is state of the art? **[8]**

b) Explain in short: Implementation of current sink and current source using MOSFET. What are the voltage compliances? How to improve them? **[8]**

Q2) Design CMOS differential amplifier for CMMR=40dB. The dissipation should not exceed 2.5 mW at supply of 2.5V. **[16]**

Q3) a) Explain in detail the concept of BGR with its necessity. **[8]**

b) Where and how the MOSFET is used as diode/Active Resistor? **[8]**

Q4) Write short notes on any three: **[18]**

a) Active Load Invertors & its parameters.
b) Techniques used in Micro Power op-amp.
c) Current amplifiers.
d) Buffered op-amps using MOSFETs.

P.T.O.

SECTION - II

Q5) a) What is MOS model? What are its objectives? How it is used by designers? **[8]**

b) In CMOS technology why do we design the size of PMOS to be higher than the nMOS? Why PMOS and NMOS are sized equally in transmission gate? **[8]**

Q6) a) What is metastability problem in digital design? How to overcome metastability? **[8]**

b) Derive an expression for Power Delay Product (PDP) and Energy Delay Product (EDP). How do PDP and EDP help CMOS designers? **[8]**

Q7) a) What are the constraints in FSM design? How to tackle them? Explain any one in detail. **[4]**

b) Design a lift controller for 3 floor building. Assume standard specifications. Draw Minimized the state diagram. Write VHDL code for the same. **[12]**

Q8) Write short notes on any three: **[18]**

a) High speed design techniques.
b) Low power design techniques.
c) CMOS parasitic.
d) CMOS layout techniques.