Total No. of Questions : 8]

SEAT No. :

P3328

[Total No. of Pages : 2

[4660]-300
M.E. (E & TC) (VLSI & Embedded Systems)
ANALOG AND DIGITAL CMOS IC DESIGN
(2008 Pattern)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates :

1) ***Answer any three questions from section - I & section - II***
2) ***Figures to the right indicate full marks.***
3) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Calculate W/L for MOSFET to offer dynamic resistance of 10 kΩ. Assume suitable data. **[8]**

b) With the help of necessary schematic explain current sink & source with Rout offered. **[8]**

Q2) Design current mirror for 100 micro A. Assume suitable data. What are the techniques to improve output resistance? Give mathematical analysis to support. **[16]**

Q3) a) What are the performance parameters of voltage reference circuit? Explore in brief. What is state of art? **[8]**

b) What is mean by buffered op-amp? Explore with the schematic? **[8]**

Q4) Write short notes on any three: **[18]**

a) Cascode amplifier

b) Macro model of op-amp

c) BGR

d) Output amplifiers

P.T.O.

SECTION - II

Q5) a) Explain with suitable example sources of static and dynamic hazards. How to eliminate static hazards? **[8]**

b) What is static and dynamic power dissipations? Derive an expression for Power Delay Product (PDP) and Energy Delay Product (EDP). **[8]**

Q6) a) What is metastability problem in digital design? How to overcome metastability? **[8]**

b) Explain domino logic in detail. **[8]**

Q7) a) Compare synchronous and asynchronous machines. **[4]**

b) Draw state diagram, write a VHDL code and test bench for 1101 Moore sequence Detector. **[12]**

Q8) Write short notes on any three: **[18]**

a) Transmission Gate: Merits, Demerits and Use.

b) Technology Scaling

c) λ Parameter and DRC

d) NORA Logic.

e) Stick Diagram and CMOS Layout