

Total No. of Questions : 8]

SEAT No. :

P4290

[Total No. of Pages : 2

[4960] - 212

M.E. (E&TC) (VLSI & Embedded Systems)

ANALOG AND DIGITAL CMOS IC DESIGN

(2008 Pattern)

Time : 3 Hours]

[Max. Marks :100

Instructions to the candidates:

- 1) *Answer any three questions from section - I & section - II.*
- 2) *Answer to the two section should be written in separate answer book.*
- 3) *Figures to the right indicate full marks.*
- 4) *Assume suitable data, if necessary.*

SECTION - I

- Q1)** a) Sketch ac-equivalent model of MOSFET. Explain how to use it as switch? Give the expression for drain current & ON resistance? [8]
b) Design current mirror to deliver $100\mu\text{A}$. Compute R_{out} ? [8]
- Q2)** a) With the help of necessary schematic explain current sink & current source with R_{out} offered? [8]
b) Draw the transistorized network of common source amplifier, common gate amplifier and common drain amplifiers. Differentiate them. [8]
- Q3)** a) With the help of suitable schematic give the expression for ratio of current in current mirror. What are the sources of ratio error? [8]
b) What is meant by buffered op-amp? Explore with the schematic. [8]
- Q4)** Write short notes on any three : [18]
a) Current references.
b) BGR.
c) Micro power op amp.
d) Macro model of op amp.

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SECTION - II

- Q5)** a) What do you mean by device parasitic & draw the high frequencies equivalent Circuit of MOSFET? [8]
b) “Generally hazards are not hazards in synchronous machines” Justify the statement. [8]
- Q6)** a) What is need of Transmission gate? Design 8:1 MUX using Transmission gate and conventional gate. [8]
b) What is active area on chip? Design CMOS logic for $F = AB + CDEF + GH$. Compute area. [8]
- Q7)** Write short notes on any three : [18]
a) NORA logic.
b) Power delay product.
c) Lambda parameter.
d) Dissipation in CMOS logic.
e) CMOS Layout techniques.
- Q8)** a) Write VHDL code for 1110 more sequence detector with state diagram. [8]
b) Compare synchronous & asynchronous machines? [8]

