Total No. of Questions : 8]

SEAT No. :

P2577

[Total No. of Pages : 2

M.E. (Semester - I)
VLSI AND EMBEDDED SYSTEMS
Analog and Digital CMOS IC Design
(2008 Pattern)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer book.***
2) ***Answer any three questions from each section.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Use of Calculator is allowed.***
6) ***Assume Suitable data if necessary.***

SECTION - I

Q1) a) What is need of voltage reference? Explain any one type of such reference circuit in detail ? **[8]**

b) What are merits of cascode arrangement? Design cascode current source for 100μA. Assume suitable data. **[8]**

Q2) a) Carry out small signal analysis of differential amplifier. Derive the equation for CMRR. **[8]**

b) What is need of low noise opamp? What are techniques to design? **[8]**

Q3) Draw FSM diagram for 10110 Mealy sequence detector, write VHDL code and test bench for it. **[16]**

Q4) Write short notes on **any three.** **[18]**

a) MOSFET as diode

b) Inverters

c) Buffered opamp

d) High speed opamp

P.T.O.

SECTION - II

Q5) a) What is concept of metastability? How to sync up? What are solutions? **[8]**

b) What is need of technology scaling? What are types? Explain any one in brief. **[8]**

Q6) a) Design CMOS logic for Y = ABC + DEFGH. Compute active area on chip. **[8]**

b) Derive the expressions for static, dynamic power dissipations and power delay product. **[8]**

Q7) a) Design latch using transmission gates. **[8]**

b) Draw top view showing metal/poly Silicon layout routing for 2 input CMOS NAND gate. Show the dimensions. **[8]**

Q8) Write short notes on **any three.** **[18]**

a) DRC rules

b) Advanced trends for ultra fast logic

c) Transient response

d) NORA logic

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