Total No. of Questions : 8] **[Total No. of Pages : 2**

P1750

[3965]-625

M.E. (E & T/C VLSI & Embedded Systems)

ANALOG & DIGITAL CMOS IC DESIGN

(2008 Course) (504181) (Sem. - I)

Time : 3 Hours] ***[Max. Marks : 100***

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) Design current mirror for 100 μA. Assume suitable data. What are the techniques to improve output resistance? Give mathematical analysis to support. **[16]**

Q2) a) What are the performance parameters of voltage reference circuit? Explore in brief. What is state of art? **[8]**

b) Design differential amplifier for voltage gain of 40 dB and bandwidth of 1MHz. **[8]**

Q3) a) List and explain in brief, device & wire parasitics normally considered while design. **[8]**

b) What is need of low voltage opamp? What are its design techniques? **[8]**

Q4) Write short notes on any three: **[18]**

a) High gain opamp.

b) Macro model of opamp.

c) BGR.

d) Cascode amplifier.

P.T.O.

SECTION - II

Q5) Draw FSM diagram, write VHDL code & test bench for 10111 mealy sequence detector. **[16]**

Q6) a) Design CMOS logic for F = AB + CDE + E (F + G). Compute area on chip. **[8]**

b) What are the constraints in FSM design? How to tackle them? Explain any one in detail. **[8]**

Q7) a) Derive an expression for power delay product. How does PDP help designer? **[8]**

b) What is λ parameter? Explain technology scaling in detail. **[8]**

Q8) Write short notes on any three: **[18]**

a) Merits, demerits & applications of transmission gate.

b) Trends in ultra fast technology.

c) CMOS layout rules.

d) NORA logic.