Total No. of Questions :8] **[Total No. of Pages : 2**

P1922

[3765]-573
M.E. (VLSI & Embedded Systems)
ANALOG & DIGITAL CMOS IC DESIGN
(2008 Course)

Time :3 Hours] ***[Max. Marks : 100***

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams should be drawn wherever necessary.***
4) ***Use of electronic pocket calculator is allowed.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explore current sink & source. What are the voltage compliances? How to improve them? **[8]**

b) Design CMOS amplifier for voltage gain of 50, band width of 100 MHz. Compute R_{out}. **[8]**

Q2) a) What are the techniques of voltage references? What are their performance parameters. **[8]**

b) What is necessity of Bandgap reference? Brief the concept with mathematical expressions. **[8]**

Q3) a) Design cascode amplifier for voltage gain of 40 dB. Compute R_{out}. Estimate bandwidth. Assume suitable data. **[8]**

b) List and explain the techniques to improve bandwidth. **[8]**

Q4) Write short notes on any three : **[18]**

a) Output amplifiers.

b) Micropower opamp.

c) Inverters & performance parameters.

d) MOSFET as active resister.

SECTION - II

Q5) Draw FSM diagram & write VHDL code for Tea/Coffee vending machine. Also write test bench assume suitable inputs & outputs. **[16]**

P.T.O.

Q6) a) Why is synchronization needed? What are the methods to achieve? **[8]**

b) What are the sources & elimination techniques of hazards? **[8]**

Q7) a) Derive the expressions for static & dynamic dissipations. Compare them w.r.t technology scaling. **[8]**

b) Design CMOS logic for F= ABCD + E (F + G). Compute area on chip. **[8]**

Q8) Write short notes on any three : **[18]**

a) MOSFET sizing.

b) Technology scaling & its effects.

c) Transmission gate & its applications.

d) NDRA logic.

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