Total No. of Questions : 8]

SEAT No. :

P4053

[Total No. of Pages : 2

[4860]-215
M.E. (E & TC) (VLSI&Embedded System)
ASIC DESIGN AND MODELING
(2008 Pattern) (Elective - I)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate answer books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Assume suitable data if necessary.***

SECTION - I

Q1) a) Write a VHDL code using structural model for the following functions: **[10]**

$F1 = AB' + A'BC$ $F2 = A' + B'$

$A3 = A \cdot B' + A' \cdot B$

b) With the help of EDA tools explain the step by step process to explain the flow of ASIC design. **[8]**

Q2) a) Differentiate between full custom and semi custom ASIC. Brief in detail the semi custom ASIC structure. **[8]**

b) Explain different post-layout verification steps with neat diagram. **[8]**

Q3) a) Draw and explain fabrication process of IC chip layout. **[6]**

b) Explain step by step process of Hardware design verification. **[10]**

Q4) Write short note on: **[18]**

a) Mixed signal design

b) Clock tree synthesis

c) Data structure for graph models

P.T.O.

SECTION - II

Q5) a) Explain w.r.t. floorplanning: **[10]**

i) Channel Capacity ii) Channel Density

iii) Channel Allocation iv) Cyclic constraints

v) Channel ordering

b) Classify routing algorithm and explain any one with neat diagram and goals, one in detail. **[8]**

Q6) a) Draw the block diagram of Design for Test and explain BIST in detail. **[8]**

b) Explain in detail zero slack algorithm for placement. **[8]**

Q7) a) Explain the term Back Annotation with goals and objectives explain VLSI Physical design flow. **[8]**

b) Explain in brief various delay models. **[8]**

Q8) Write short note on: **[18]**

a) Static timing Analysis

b) Fault Simulation

c) EDA tools.