Total No. of Questions : 8]

SEAT No. :

**P2783**

[Total No. of Pages :2

# [4660] - 303
# M.E. (E & TC) (VLSI and Embedded System)
# a - ASIC DESIGN AND MODELLING
# (2008 Course) (Elective - I) (504184) (Semester - I)

*Time : 3 Hours]* *[Max. Marks : 100*

***Instructions to the candidates:***

1) ***Question no.1 and Question no. 8 are compulsory.***
2) ***Answer any two questions from remaining questions from each Section.***
3) ***Answers to the two sections should be written in separate answer books.***
4) ***Neat diagrams must be drawn wherever necessary.***
5) ***Figures to the right indicate full marks.***
6) ***Use of electronic calculator is allowed.***
7) ***Assume suitable data, if necessary.***

## SECTION - I

***Q1)*** a) Explain the step by step process of ASIC design in detail. Brief about the various EDA tools that are used for this process. **[12]**

b) Describe the various issues in verification. **[6]**

***Q2)*** a) Design the smart Engineering building lift controller such that: **[8]**

Input : in _button (10 downto 0), position_sensor (15 downto 0)

Outputs: up_down, stop_go, door_open_close, display (10 downto 0)

Additional input/outputs: over_weight, beep

How many states, processes do you need?

Draw the state transition diagram.

Write VHDL code.

b) Describe the various verification issues. **[8]**

***Q3)*** a) Compare the hardware design verification and software design verification. **[8]**

b) Draw the stick diagram for 2 inputs AND gate. Calculate area needed on chip. **[8]**

***P.T.O.***

***Q4)*** a) What do you mean by clock skew? How it can be rectified? Explain it with neat waveforms. **[8]**

b) List different DFT techniques and explain in detail with example.

memory BIST Insertion Technique. **[8]**

## SECTION - II

***Q5)*** a) What are the goals of placement and explain the Eigen value algorithm for placement? **[10]**

b) What are the objectives of system portioning and explain in detail the group migration algorithm in for system partitioning. **[6]**

***Q6)*** a) Explain static timing analysis in detail. **[8]**

b) Explain the K-L algorithm in detail. **[8]**

***Q7)*** a) What are various issues in analog mixed signal design? **[8]**

b) Explain the various routing techniques. Explain any one of them in detail. **[8]**

***Q8)*** Write short note on: **[18]**

a) Power dissipation.

b) Post layout synthesis.

c) Automatic test pattern generator [ATPG].