[4460] - 233

M.E. (E&TC) (VLSI Embedded System)
ASIC DESIGN AND MODELLING
(2008 Pattern) (Semester - I) (Elective - I (a))

Time :3 Hours]   *[Max. Marks : 100*

Instructions to the candidates:-

1) *Answer any three questions from each section.*
2) *Answers to the two sections should be written in separate books.*
3) *Neat diagrams must be drawn wherever necessary.*
4) *Figures to the right indicate full marks*
5) *Assume suitable data, wherever necessary.*

SECTION - I

Q1) a) Explain the step by step process of ASIC design. Brief about the various EDA tools that are used in this process. **[12]**

   b) Describe the various issues in verification. **[6]**

Q2) a) Design the smart lift controller such that :- **[10]**

   Input :- in_button (10 down to 0), position_sensor (15 down to 0), 01P: up_down, stop - go, door-open-close, display (10 down to 0).

   Addition i/p & 01Ps:- over weight, beep

   How many states, processes do you need?

   Draw state transition diagrams. Write VHDL code.

   b) Write short note on semi custom ASIC design. **[6]**

Q3) a) What are the goals and objectives of placement. Explain in detail. **[8]**

   b) Draw the stick diagram for 3 i/p AND gate. Calculate area needed on chip.**[8]**

Q4) a) What are the vatious methods to reduce clock skew. Explain in brief. **[8]**

   b) List different DFT techniques and explain in detail by giving example of memory BIST insertion technique. **[10]**

SECTION - II

Q5) a) Explain the significance of Eigen values in placement algorithm. **[10]**

   b) Explain in detail the group migration algorithm for system partitioning.**[8]**

Q6) a) Explain static timing analysis. **[8]**

   b) Explain K-L algorithm in detail. **[8]**

Q7) a) What are the various routing techniques explain any one in detail. **[8]**

b) Explain the significance of scan path technique for testing sequential circuits. **[8]**

Q8) Write short note on. **[18]**

a) Power dissipation

b) Pre layout and post layout synthesis.

c) Automatic test pattern generator.

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