Nov - Dec - 2012

Total No. of Questions : 8]

SEAT No. :

P1567

[Total No. of Pages : 2

[4265] - 661

M.E. (E & TC) (VLSI & Embedded System)

ASIC DESIGN & MODELLING

(2008 Course) (Elective - I(a)) (Semester - I)

Time :3 Hours] *[Max. Marks :100*

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data, if necessary.***

SECTION – I

Q1) a) Explain the different type of modelling used in VHDL with respect to different constraints. **[6]**

b) Write a VHDL code for four bit Universal shift register. **[12]**

Q2) a) Draw and explain the ASIC design flow. **[8]**

b) Explain the block diagram of synthesis in detail and explain the technology library used in synthesis. **[8]**

Q3) a) Find the minimal test set for the circuit shown in fig. a. to show the coverage of various stuck at 1 for all possible tests. **[8]**

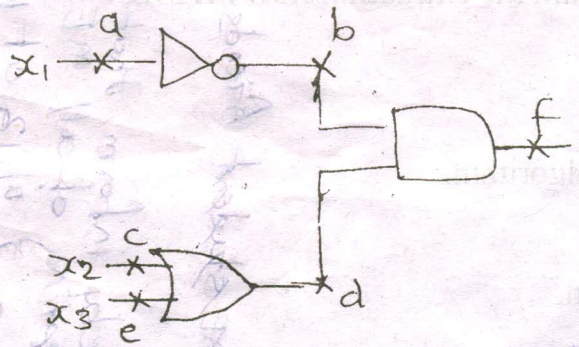

fig a

P.T.O.