Total No. of Questions : 8]

SEAT No. : ____

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M.E. (E&TC) (VLSI & Embedded System)

ASIC DESIGN AND MODELING

(2008 Pattern) (Elective - I)

Time : 3 Hours] ***[Max. Marks :100***

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain with flow diagram the working of ASIC Design flow. **[10]**

b) With neat diagram, describe the structure of semi custom ASIC. **[8]**

Q2) a) Classify simulation techniques. Explain in detail static timing analysis. **[8]**

b) What are different modeling techniques? Write a VHDL code for 4:1 multiplexer using behaviour modeling methods. **[8]**

Q3) a) Describe with neat block diagram, the terms constraints and Attributes in detail required for synthesis process. **[8]**

b) Compare Hardware design and software design verification strategy for ASIC. **[8]**

Q4) Write short notes on : **[18]**

a) EDA tools for ASIC design.

b) Verification Issues in ASIC construction.

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SECTION - II

Q5) a) List objectives of physical design block in ASIC. **[10]**

b) Define the following terms : **[8]**

i) Fault coverage

ii) Controllability

iii) Observability

Q6) a) Describe in detail memory BIST insertion DFT technique for fault detection. **[8]**

b) List out various design rule and electric rule checks in ASIC flow. **[8]**

Q7) a) Explain in detail, algorithm for system partitioning. **[8]**

b) Describe the significance of eigen value algorithm for placement in physical design. **[8]**

Q8) Write short notes on : **[18]**

a) Tools for PAR.

b) Fault simulation.

c) Graph models.

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