Total No. of Questions : 6]

SEAT No. :

P3959

[Total No. of Pages : 2

[4760]-281

M.E. (E & TC) (VLSI & Embedded System)

ASIC DESIGN AND MODELING

(2008 Course) (Semester - I) (Elective - I) (504184)

Time : 3 Hours] *[Max. Marks :100*

Instructions to the candidates:

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Assume suitable data if necessary.***
3) ***All questions are compulsory.***

SECTION - I

Q1) a) With neat diagram, explain the working of ASIC design flow. **[8]**

b) Write a short note on modeling combinational and sequential circuits. **[10]**

Q2) a) List verification issues. Explain in detail the working of hardware and software design verification. **[8]**

b) Explain with neat diagram, hardware modeling with VHDL. Give one example in detail. **[8]**

Q3) a) Write a brief note on verification strategy of complex logic design model. **[8]**

b) Classify and explain in brief different ASIC construction. **[8]**

SECTION - II

Q4) Write a short note on **[18]**

a) Static timing analysis.

b) Clock Tree synthesis.

P.T.O.

Q5) a) List different objectives of physical verification. **[8]**

b) What are different goal of system partitioning explain one algorithm in detail. **[8]**

Q6) a) With neat example, explain stick diagram by using CMOS for various combination. **[8]**

b) List out features of tools used for front to back end chip design. **[8]**

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