Total No. of Questions : 8]

SEAT No. :

P2877

[Total No. of Pages : 2

M.E. (E & TC) (VLSI and Embedded System) (Semester - I)

ASIC DESIGN AND MODELING

(2008 Pattern) (Elective - I)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Question 1 and 5 are compulsory. Out of remaining attempt any 2 question from Section 1 and 2 questions Section -II.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Use of Calculator is allowed.***
6) ***Assume Suitable data if necessary.***

SECTION -I

Q1) a) Explain ASIC design flow in detail. List different EDA tools used for ASIC design. **[7]**

b) Draw the FSM diagram for traffic light controller and write VHDL code for the same. Assume suitable data **[7]**

Q2) a) What do you mean by clock skew? How it can be rectified? Explain it with neat wave forms. **[9]**

b) What is necessity of timing analysis? Explain in detail static timing analysis. **[9]**

Q3) a) List the goals and objectives for each of the ASIC physical design step. **[9]**

b) Describe the various verification issues in detail. **[9]**

Q4) a) Explain the scan path technique in detail. **[9]**

b) Explain TAP controller in detail. **[9]**

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SECTION - II

Q5) a) Describe the layout planning? How automatic layout planning plays important role in CMOS fabrication. **[7]**

b) List different fault models present. Explain in detail stuck at fault models. **[7]**

Q6) a) Explain power analysis in detail. How it can be categorized? Where it is useful? **[9]**

b) Discuss the power analysis in detail. **[9]**

Q7) a) Compare hardware design verification and software design verification. **[9]**

b) What are the analog mixed signal design issues? Explain in brief. **[9]**

Q8) Write short note on

a) DRC&ERC **[6]**

b) Automatic test pattern generation **[6]**

c) Power grid analysis **[6]**

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