

Total No. of Questions : 8]

SEAT No. :

P2104

[Total No. of Pages : 2

[4460] - 244

M.E. (E & TC) (VLSI & Embedded System) (Semester - II)

ADVANCED DIGITAL SYSTEM DESIGN

(2008 Pattern) (Elective - III(c))

Time : 3 Hours]

[Max. Marks : 100

Instructions to the candidates:

- 1) *Answer any three questions from each section.*
- 2) *Answers to the two sections should be written in separate books*
- 3) *Neat diagrams must be drawn wherever necessary.*
- 4) *Figures to the right indicate full marks.*
- 5) *Assume suitable data, if necessary.*

SECTION - I

- Q1)** a) Explain in detail the datapath architecture of a simple CPU. [8]
b) Draw a neat block diagram of the micro-programmed control unit and explain it in detail. [8]
- Q2)** a) What is a hazard? Explain static and dynamic hazards and also discuss how hazard free circuits can be designed. [8]
b) Find a hazard-free minimum cost POS implementation of the function.
$$f(x_1, \dots, x_4) = \pi M(0, 2, 3, 7, 10) + D(5, 13, 15)$$
 [8]
- Q3)** a) Explain the terms “reliability” and “MTBF”. Also discuss how the reliability of a digital system can be estimated. [8]
b) Discuss how asynchronous inputs can be handled in a digital system. Also explain how the problem arising due to use of two or more synchronizers can be avoided. [8]
- Q4)** Write notes on : [18]
a) Clock skew.
b) ATM packet generator.
c) RISC CPU.

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SECTION - II

- Q5)** a) What is Stuck-at fault? Explain how path sensitization can be used to test stuck-at faults in combinational circuits. [8]
b) What is boundary Scan? Explain the basic boundary Scan architecture. [8]
- Q6)** a) Model a $2K \times 8$ static RAM using VHDL. [8]
b) Explain in detail the 486 bus model. [8]
- Q7)** a) With the help of a neat flowchart explain the procedure required to carry out floating point addition. [8]
b) Draw and explain the fraction multiplier circuit used in a floating-point multiplier. [8]
- Q8)** Write notes on : [18]
a) Asynchronous communication.
b) BIST.
c) Testing sequential circuits.

