Total No. of Questions : 8]

SEAT No. :

P4302

[Total No. of Pages : 2

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M.E. (E&TC) (VLSI & Embedded System Design)

ADVANCED DIGITAL SYSTEM DESIGN

(2008 Pattern) (Elective - III) (Semester - II)

Time : 3 Hours] *[Max. Marks :100*

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate answer-books.***
3) ***Figures to the right indicate full marks.***
4) ***Neat diagrams must be drawn wherever necessary.***
5) ***Assume suitable data if necessary.***

SECTION - I

Q1) a) Describe the design issues of RISC processors. **[8]**

b) Draw and explain the memory interfacing with microprocessor. **[10]**

Q2) Consider the following logic function.

$F(A, B, C, D) = \Sigma m(0, 4, 5, 10, 11, 13, 14, 15)$

a) Find the two different minimum circuits which implement F using AND and OR gates. Identify two hazards in each circuit. **[8]**

b) Find an AND-OR circuit for F which has no hazards. **[4]**

c) Find an OR-AND circuit for F which has no hazards. **[4]**

Q3) a) Explain the Self test circuit for RAM with signature register. **[6]**

b) Draw address and data path architecture of CPU, indicate names of various blocks. Which unit of CPU sequences the data path operation? How are they implemented? **[10]**

Q4) a) Design a sequence detector in which output is '1' only if the input sequence of 10100 occurs at consecutive clock pulses. **[8]**

b) What do you meant by clock skew? Explain the methods to minimize the clock skew. **[8]**

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SECTION - II

Q5) a) Model 4K × 8 Dual port RAM using VHDL. **[8]**

b) Draw $2^m \times n$ array of DRAM cells and explain operation in detail. **[8]**

Q6) a) What are the major steps to design ATM packet generator? Explain in detail. **[8]**

b) Explain ATM Switch architecture using block diagram. Discuss important steps for design of ATM switch. **[8]**

Q7) a) What is PBRS generator? Draw and explain a scheme to generate PRBS. **[8]**

b) With neat flowchart, explain steps in floating point addition. **[8]**

Q8) Write notes on : **[3 × 6 = 18]**

a) IEEE 486 BUS.

b) Boundary scan.

c) State machine for TAP Controller.

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