Nov - Dec - 2011

[4063] – 343

T.E. (Computer Engineering) (Semester – I) Examination, 2011
MICROPROCESSORS AND MICROCONTROLLERS
(2008 Pattern) (New)

Time : 3 Hours Max. Marks : 100

Instructions : *1) In Section **I**, attempt Q. No. **1** or Q. No. **2**, Q. No. **3** or Q. No. **4**, Q. No. **5** or Q. No. **6**.*
*2) In Section **II**, attempt Q. No. **7** or Q. No. **8**, Q. No. **9** or Q. No. **10**, Q. No. **11** or Q. No. **12**.*
*3) Answers to the **two** Sections should be written in **two separate** books.*
*4) **Neat** diagrams must draw **wherever** necessary.*
*5) Figures to the **right** indicate **full** marks.*
*6) Assume **suitable** data **if necessary**.*

SECTION – I

1. a) What is the function of each of the following pins ? 6
   i) $\overline{\text{AZOM}}$ ii) PWT iii) INJT

   b) With the help of neat diagram explain architecture of pentium processor. 8

   c) Describe on chip cache organisation of pentium. 4

OR

2. a) Describe the floating point unit in pentium. 6

   b) Which features makes pentium, a superscalar processor ? Explain in detail. 6

   c) What is the function of prefetch buffer and Branch target buffer in pentium processor ? 6

3. a) How pipelined bus cycles are different than non-pipelined bus cycles ? Explain with timing diagram. 6

   b) Describe different addressing modes of pentium with suitable examples. 6

   c) Describe following instructions. 4
   i) XADD ii) SWAPB iii) BTC iv) WBINVD

OR

P.T.O.

4. a) Draw and explain timing diagram of non-pipelined read bus cycle of pentium. **8**

   b) What is the purpose of control registers ? Explain significance of CRO in working of cache and paging unit. **8**

5. a) Describe call gate mechanism in details. Draw the related descriptor formats. **8**

   b) Describe logical to linear address translation mechanism in pentium. Draw the required data structures. **8**

OR

6. a) What are privilege level checks performed by pentium when FAR JMP or FAR CALL instruction is executed ? Under what circumstances privilege level is changed by pentium ? Explain with the help of diagram. **8**

   b) How pages can be protected in pentium ? Give details. **8**

SECTION – II

7. a) What are contents of TSS ? Discuss the use of TSS in multitasking ? **8**

   b) What is I/O permission bit map ? Under what circumstances is it referred by pentium ? **6**

   c) Differentiate between real mode and virtual mode. **4**

OR

8. a) How interrupts are handled in protected mode ? Explain with the help of neat diagram. **8**

   b) What is difference between interrupt, Fault, Trap and Abort ? **6**

   c) Explain nested task in pentium. **4**

9. a) What are different addressing modes in 8051 ? Explain with suitable example. **8**

   b) Draw the memory map of 8051 microcontroller. What is bit addressable area ? How many bits are addressable ? What are uses of SFRs ? **8**

OR