Total No. of Questions—**12**] [Total No. of Printed Pages—**4+1**

Seat No.	

[4657]-72

S.E. (Computer/I.T.) (First Semester) EXAMINATION, 2014

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** (*i*) Answers to the two Sections should be written in separate answer-books.

(*ii*) Answer any *three* questions from each Section.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Use of calculator is allowed.

(*vi*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Convert the following Hexadecimal numbers into their equivalent binary, decimal and octal numbers : [12]

(*i*) A72E

(*ii*) BD6.7

(*iii*) 0.BF85

(*iv*) DF.

P.T.O.

(*b*) Perform the following BCD Addition; also represent the answer in valid BCD : [6]

(*i*) 7+1

(*ii*) 7+4

(*iii*) 9+8.

Or

2. (*a*) Express the following numbers in binary format. Write step by step solution : [6]

(*i*) $(762)_{\text{octal}}$

(*ii*) $(246)_{\text{decimal}}$

(*iii*) $(1101.11)_{\text{decimal}}$

(*b*) Solve the following equations using corresponding minimization techniques : [12]

(*i*) $Z = f(A, B, C, D) = \Sigma m(0, 2, 5, 6, 8, 10, 13, 15)$

(*ii*) $Z = f(A, B, C, D) = \Pi M(4, 5, 6, 7, 14, 15)$.

3. (*a*) Solve by Quine-McClusky technique : [10]

$Z = f(A, B, C, D) = \Sigma(0, 1, 3, 7, 8, 9, 11, 15)$.

(*b*) Explain standard TTL characteristics in brief. [6]

Or

4. (*a*) Draw 2-i/p 2 input CMOS NAND gate. [8]

(*b*) Compare TTL and CMOS logic family. Also draw CMOS-NOR gate. [8]

5. (*a*) Design and implement BCD to Excess-3 code converter using logic gates. Starting with truth table show K-maps and circuit diagram of your design. [8]

(*b*) Design and implement 3-bit an Even Parity Generator and Checker. [8]

Or

6. (*a*) Design and implement the following equation using single 8 : 1 multiplexer :

$$F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 15).$$

Explain the truth table of your circuit in short. [8]

(*b*) Design and implement two bit comparator using basic gate only. [8]

SECTION II

7. (*a*) With the help of internal block diagram explain how counter IC 7490 can be used as : [8]

(*i*) BCD counters

(*ii*) MOD-6 counter.

(*b*) How will you convert JK flip-flop into D flip-flop and T flip-flop ? Explain application of D and T flip-flop in sequential circuits ? [10]

Or

8. (*a*) What is the difference between Asynchronous and Synchronous Counter ? Draw and explain 3 bit Synchronous Up-Down counter, also draw necessary timing diagram. [10]

(*b*) Design the following sequence generator using T flip-flops. Use synchronous counter. Design methodology 0 — 1 — 7 — 4 — 2 — 0 and repeats. [8]

9. (*a*) What is ASM chart ? Design ASM chart for 3-bit Up-Down counter. [8]

(*b*) Write VHDL code for Half Adder in Structural and Dataflow modeling. [8]

Or

10. Draw ASM chart for the following state machine :

A two bit counter with output 'Q1 Q0' and enable signal 'X' is to be designed. If X = 0, Counter changes the state as '00—01—10—00'. If X = 1, Counter should remain in the present state. Design circuit using JK ff and suitable MUX. [16]

11. (*a*) Draw and explain structural diagram of CPLD and FPGA. Also explain difference between the two types of devices. [8]

(*b*) Implement 4 : 1 MUX using suitable PAL. [8]

Or

12. (*a*) What is Bus ? Explain in brief different types of Bus used by a Microprocessor. [8]

(*b*) With a neat block diagram explain microprocessor architecture. [8]