Total No. of Questions—**12**] [Total No. of Printed Pages—**4+2**

Seat No.	

[4457]-113

S.E. (Computer/I.T.) (First Semester)

EXAMINATION, 2013

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** (*i*) Attempt Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6** from Section I and Q. No. **7** *or* Q. No. **8**, Q. No. **9** *or* Q. No. **10**, Q. No. **11** *or* Q. No. **12** from Section II.

(*ii*) Assume suitable data, if necessary.

(*iii*) Figures to the right indicate full marks.

SECTION I

1. (*a*) Minimize the following functions and realize using only one types of gates : [10]

$F_1(A, B, C, D) = \Sigma m\ (0, 1, 3, 7, 8, 9, 11, 15)$

$F_2(A, B, C, D) = \Sigma m\ (0, 1, 2, 3, 5, 7, 8, 10, 12, 13, 15)$

P.T.O.

(*b*) Represent the following numbers in binary and octal codes :

(*i*) $(27)_{10}$

(*ii*) $(396)_{10}$

(*iii*) $(15)_{16}$

(*iv*) $(7F)_{16}$ [8]

Or

2. (*a*) Minimize the following function and realized using minimum number of logic gates :

F_1 (A, B, C, D) = Σm (0, 5, 10, 15)

F_2 (A, B, C, D) = Σm (0, 1, 2, 5, 6, 7) [10]

(*b*) Represent the following numbers in decimal and hexadecimal codes :

(*i*) $(1111)_2$

(*ii*) $(23)_8$

(*iii*) $(111001111)_2$

(*iv*) $(456)_8$ [8]

3. (*a*) Differentiate between standard TTL and CMOS Logic circuit w.r.t. : [8]

(*i*) FANOUT

(*ii*) Propagation Delay

(*iii*) Power Dissipation

(*iv*) Figure of merit

(*v*) Noise Margin

(*vi*) Voltage and current parameter

(*vii*) Power supply requirement

(*viii*) Application

(*b*) Draw and explain the working of 2-input CMOS NAND Gate. [8]

Or

4. (*a*) Differentiate between Totem pole and open collector output configuration in TTL circuit. [4]

(*b*) Explain the meaning of the following symbol used in 5474 series TTL IC's : L, H, AS, ALS. [4]

(*c*) In 2-input TTL NAND gate with totem pole output configuration. What happen if :

(*i*) R_p (Pull-up Register) = 0 ?

(*ii*) Diode D is not present ?

(*iii*) Output accidently get shorted to ground ? [8]

5. (*a*) Design a Excess 3 to BCD code converter using minimum number of logic gates. Show truth table-maps and logic diagram of your design. [8]

(*b*) Design a Full adder circuit using 8 : 1 Multiplexer. [8]

Or

6. (*a*) Design 3-bit binary to 3-bit gray code converter circuit using IC-74138. [8]

(*b*) Design 4-bit BCD adder using binary adder ICS. [8]

SECTION II

7. (*a*) Design a sequential circuit using Mealy machine to detect the sequence.....1001.....(Use JK flip-flop) [10]

(*b*) Write short notes on :

(*i*) IC-7476

(*ii*) IC-7490 [8]

Or

8. (*a*) Design a 3-bit Asynchronous UP/DOWN counter using Mode control input M (Use JK flip-flop) consideration :

(*i*) If M = 0; Down counting

(*ii*) If M = 1; UP-counting [10]

(*b*) Perform the following conversion :

(*i*) S-R flip-flop to J-K flip-flop

(*ii*) D flip-flop to T flip-flop [8]

9. (*a*) What is ASM chart ? Explain ASM techniques to designing the sequential circuits in detail. Compare ASM chart and state diagram. [8]

(*b*) Write a VHDL code for toggle (T) flip-flop with asynchronous reset. [8]

Or

10. (*a*) A sequential circuit has to COUNT UP from 0 to 3. The circuit also has a control input M. If M = 0, the circuit will remain in the current state and if M = 1, the circuit will go to the next state. Draw the ASM chart. Also design the circuit with the help of D flip-flops. [8]

(*b*) Explain the difference between concurrent and sequential statement in VHDL. [4]

(*c*) Write a short note on signal and variable in VHDL. [4]

11. (*a*) What is PLD ? Design a 2 : 4 decoder using PLD. [8]

(*b*) Explain the functions of the following in microprocessor :

(*i*) Address Bus

(*ii*) ALU

(*iii*) Stack pointer

(*iv*) Instruction register [8]

Or

12. (*a*) What do you mean by configurable devices ? Differentiate between PLA and PAL. [8]

(*b*) Draw and explain the architectures of FPGA. [8]