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Total No. of Questions—12]

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[3862]-213

S.E. (Comp. Engg.) (First Semester) EXAMINATION, 2010

(Common to Computer and I.T.)

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 COURSE)

Time : Three Hours

Maximum Marks : 100

N.B. :— (i) Answer Q. No. 1 or 2, Q. No. 3 or 4, Q. No. 5 or 6 from Section I and Q. No. 7 or 8, Q. No. 9 or 10, Q. No. 11 or 12 from Section II.

(ii) Answers to the two sections should be written in separate answer-books.

(iii) Neat diagrams must be drawn wherever necessary.

(iv) Figures to the right indicate full marks.

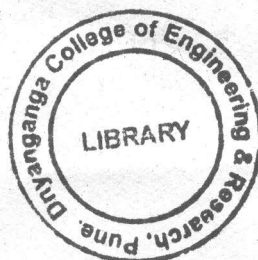
### SECTION I

1. (a) Design and explain in detail 4-bit input grey code to 7-segment BCD code conversion technique. For this design use K-map reduction and MSI circuit for each segment of display. [16]
- (b) Enlist various code conversion methods. [2]

Or

2. (a) Express the following numbers in binary format. Write step by step solution. [12]

(i)  $(7762)_{\text{octal}}$



P.T.O.

(ii)  $(432A)_{\text{hex}}$

(iii)  $(2946)_{\text{decimal}}$

(iv)  $(1101.11)_{\text{decimal}}$ .

(b) What will max. 4-digit equivalent Hex number for 4-digit max. Decimal number ? Also perform the following subtraction : [6]

$$(7048)_{\text{Decimal}} - (07A8)_{\text{Hex.}}$$

3. (a) Solve the following using K-map reduction technique. Also draw MSI circuit for output. [12]

(i)  $Z = f(A, B, C, D) = \pi (1, 2, 3, 9, 10, 12, 15)$

(ii)  $Z = f(A, B, C, D) = \pi (0, 2, 3, 4, 6, 8, 11, 13).$

(b) Explain for IC 74LSXX various characteristics in brief. [4]

Or

4. (a) Draw and explain the design of 3-I/P TTL NAND gate circuit. Also explain various I/P, O/P states and corresponding transistor (ON/OFF) states. [12]

(b) Explain working of 2-input CMOS-NOR gate. [4]

5. (a) Explain the working of cascaded mode magnitude comparator IC 7485. [8]

(b) Draw and explain 4-bit BCD adder using IC 7483. Also explain with reference to your design addition of  $(9 + 5)_{\text{BCD}}$  and

$(7 + 2)_{\text{BCD}}$ . [8]

