UNIVERSITY OF PUNE

[4362]-213

S. E. (Computer and I.T) Examination - 2013

Digital Electronics and Logic Design

(2008 Pattern)

Total No. of Questions : 12 **[Total No. of Printed Pages :3]**

[Time : 3 Hours] **[Max. Marks : 100]**

Instructions :

(1) Answer Q1 or Q2, Q3 OR Q4, Q5 OR Q6, From section I and Q7 OR Q8, Q9 OR Q10, Q11 OR Q12 From section II.

*(2) Answers to the **two sections** should be written in **separate answer-books**.*

(3) Neat diagrams must be drawn wherever necessary.

(4) Black figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

SECTION-I

Q1.

a) With the help of Quine-McCluskey method, determine the prime implicants for the following equation:
$F(A,B,C,D) = \sum m(0,1,2,5,6,7)$ [8]

b) Convert the following decimal numbers into their equivalent hexadecimal numbers and octal numbers.
(1) 936 (2) 1507 (3) 23.56 (4) 1.025 (5) 100.5 [10]

OR

Q2.

a) Minimize the following functions and realize using minimum number of logic gates.
$F_1 = \sum m(0,3,5,6,9,10,12,15)$
$F_2 = \sum m(0,1,2,3,11,12,14)$ [8]

b) Convert the following hexadecimal numbers into their equivalent octal numbers and binary numbers.
(1) A72E (2) BD6.7 (3) 0.AF54 (4) DF (5) FF [10]

Q3.

a) Explain the standard TTL characteristics in detail [8]

b) Draw and explain the working of 2-input CMOS NOR gate. [8]

OR

Q4.

a) Why is it necessary to interface between TTL and CMOS? Draw and explain the circuit arrangement of interfacing CMOS gate to number of TTL gates. [8]

b) Explain with the help of circuit diagram 2-input TTL NAND gate with Totem Pole output driver [8]

Q5.

a) Design and implement BCD to Excess-3 code converter using dual 4:1 multiplexers and some logic gates. [8]

b) Design 8-bit comparator using IC-7485 [8]

OR

Q6.

a) Design and implement BCD to Excess-3 code converter using required logic gates. Show truth table K-maps and circuit diagram of your design [8]

b) Draw and explain 4-bit BCD subtractor using IC 7483. Explain the operation on BCD numbers: 5-7. [8]

SECTION-II

Q7.

a) What is MOD counter? Draw the internal structure of IC 7490. Design MOD 56 counter using IC 7490 & necessary logic gates. [10]

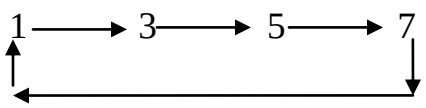
b) Draw and explain the working of master slave JK flip flop. Draw excitation table of JK flip flop. [8]

OR

Q8.

a) Design sequence detector to detect a sequence of 101011. Use JK flip flop in design. Draw the necessary state diagram, state table and logic diagram of you design. [10]

b) What is lock out condition? Design sequence generator using JK FFs. Avoid lockout condition. [8]



Q9.

a) What is ASM chart? State and explain the basic components of ASM Chart. Mention application of ASM chart. [8]

b) Write the VHDL code for full adder in structural and data flow modeling styles. [8]

OR

Q10.

a) Draw an ASM chart for the 3-bit down counter having one enable line such that:
E=1 (counting enabled)
E=0 (counting disabled)
Also draw the state diagram. [8]

b) Explain the following statements used in VHDL with suitable examples:
(1) Process (2) case (3) If then Else (4) Signal assignment [8]

Q11.

a) Explain the functions of following in microprocessor:
(1) ALU (2) Program counter (3) stack pointer (4) instruction register [8]

b) Implement the following functions using PLA: [8]
$F_1(A, B, C) = \sum m(1,2,4,6)$
$F_2(A, B, C) = \sum m(0,1,6,7)$

OR

Q12.

a) Explain in brief the functions of address bus, Data bus and control bus for a basic microprocessor, [8]

b) Draw and explain basic architecture of FPGA state difference between PLA and FPGA [8]