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Total No. of Questions—12] [Total No. of Printed Pages—4

Seat No.	

[4262]-209

S.E. (Comp. Engg.) (II Sem.) EXAMINATION, 2012

COMPUTER ORGANISATION

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer any *three* questions from each Section.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Show the general structure of an IAS computer (stored program computer) and explain. [8]

(*b*) Explain instruction cycle with the help of state diagram. [10]

Or

2. (*a*) Explain Booth's algorithm to multiply the following pair of numbers : [10]

A = 13 multiplicand

B = –11 multiplier

P.T.O.

(*b*) Give the steps involved in non-restoring division with an example. [8]

3. (*a*) With the help of diagram explain internal structure of CPU. [8]

(*b*) Describe the following addressing modes along with suitable examples : [8]

(*i*) Indirect

(*ii*) Register indirect

(*iii*) Base with Index

(*iv*) Direct.

Or

4. (*a*) What are the advantages of pipelining ? [8]

(*b*) What is the difference between data hazard and instruction hazard ? Given an example of each. [8]

5. (*a*) What are the differences between the single and multiple bus organization of the control unit ? [8]

(*b*) How are the control signals generated in hardwired control unit ? [8]