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Seat No.	
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[4757]-189

S.E. (Computer Engineering) (Second Semester)

EXAMINATION, 2015

COMPUTER ORGANIZATION

(2008 PATTERN)

Time : Three Hours

Maximum Marks : 100

- N.B. :-**
- (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6 from Section I.
 - (ii) Answer Q. No. 7 or Q. No. 8, Q. No. 9 or Q. No. 10, Q. No. 11 or Q. No. 12 from Section II.
 - (iii) Neat diagram must be drawn wherever necessary.
 - (iv) Figures to the right indicate full marks.
 - (v) Assume suitable data, if necessary.

SECTION I

1. (a) Draw the hardware implementation of booth's algorithms and explain the same. [8]
- (b) Show the general structure of IAS computer. Explain stored program concept. [6]
- (c) Write neat diagram, explain in detail functional units of computer system. [4]

P.T.O.

Or

2. (a) Perform the following divisions using restoring division : [8]
(i) Dividend = 1011
(ii) Divisor = 11.
- (b) Draw and explain the flowchart for floating point addition and explain. [6]
- (c) Draw and explain Von Neumann architecture. [4]
3. (a) Draw and explain CPU architecture of Intel processor. [8]
(b) Discuss in detail register organization of intel processor. [8]

Or

4. (a) List and explain different addressing modes of Pentium processor. [8]
(b) Explain in detail horizontal and vertical organization of microinstructions. [8]
5. (a) What are the different design methods for hardwired control units ? Explain any *one*. [8]
(b) Explain the design of ALU using combinational circuits. [8]

Or

6. (a) Draw and explain single bus organization of CPU. [8]
(b) Explain instruction cycle. How will you represent instruction cycle with interrupts ? Explain. [8]

SECTION II

7. (a) What is virtual memory concept ? Explain the role of TLB in virtual memory organization. [10]
(b) Explain the following : [8]
(i) RAID
(ii) Magnetic Memory.

Or

8. (a) Explain cache coherence strategies. [8]
(b) Explain the following : [10]
(i) DAT
(ii) DRAM.
9. (a) Explain Synchronous and Asynchronous bus in an input operation with timing diagrams. [8]
(b) Explain Programmed I/O and Interrupt Driven I/O. [8]

Or

10. (a) Explain in detail DMA data transfer mode. [8]
(b) Explain in detail how scheduling and memory management is done by operating system with its types. [8]
11. (a) Explain in detail super scalar architecture. [8]
(b) Explain Symmetric multiprocessor organization. [8]

Or

12. (a) Enlist the characteristics of Non-Uniform Memory Access (NUMA). [8]
(b) Compare RISC versus CISC. [8]