Total No. of Questions : 6]

SEAT No. :

P3072

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[4660] - 1266
M.E (Computer)
ADVANCED COMPUTER ARCHITECTURE
(2013 Course) (510103) (Semester - I)

Time : 3 Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***All questions are compuslory.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Assume Suitable data if necessary.***

Q1) a) Describe the four variants of PRAM model and compare it with parallel computer architectures. **[5]**

b) State the concept of fine grain and coarse grain scheduling. How the grain size affects on the parallelism observed in multiprocessor systems? **[4]**

OR

a) State the following terms w.r.t parallelism and dependence relations: **[5]**

i) Communication latency

ii) flow dependence

iii) Antidependance

iv) Output dependence

v) Resource dependence

b) State and define the routing functions of Mesh and Hypercube Interconnection Network. **[4]**

Q2) a) How Flynn has classified parallel computers? Why MISD architecture does not exist? **[4]**

b) State briefly the standard measures adopted by Industry to compare the performance of parallel computer systems. **[4]**

OR

P.T.O.

a) What is Scalability? State the various metrics used to define the scalability. **[4]**

b) Derive the Gustafson's law for speedup performance. How is it different than Amdahl's law? **[4]**

Q3) a) State and obtain the performance of a k-stage pipeline processor handling n instructions w.r.t following parameters- **[4]**

i) Speedup ii) Efficiency iii) Throughput

b) Discuss the address translation mechanism for a system supporting paging mechanism. **[4]**

OR

a) State the 4-level memory hierarchy defined for a computer system. How the data transfer takes place between adjacent levels of a memory hierarchy? **[4]**

b) Explain in brief , the use of Reservation stations and Hardware scoreboarding for dynamic instruction scheduling in pipeline processors. **[4]**

Q4) a) What are the multi-threaded architectures? Discuss the various performance parameters of multi-threaded processor architectures. **[4]**

b) What are the cache write policies used for cache updating? With state diagram explain the Write Invalidate cache coherency protocol. **[4]**

OR

a) With block diagram explain the architecture of multivector multiprocessor. **[4]**

b) What is data parallel programming? Compare between SPMD and MPMD programming. **[4]**

Q5) a) Explain with example the use of synchronization primitives in parallel programming. **[4]**

b) Compare PVM with MPI Message passing libraries. **[4]**

OR

a) What do you mean by implicit and explicit parallel programming? Compare between synchronous and asynchronous message passing. **[4]**

b) State the standard constructs and complier directives used in High Performance Fortran (HPF) or Fortan - 90 as a data parallel programming language. **[4]**

Q6) a) Explain the Three Tier architecture of cloud computing. **[5]**

b) Discuss important features of Quantum computing. How these architectures can be used for distributed parallel processing. **[4]**

OR

a) State the following terms w.r.t. Grid computing. **[5]**

i) Middleware

ii) OGSA

iii) OGSI

b) Explain different services offered by Cloud. What is the difference between public and private cloud? **[4]**