Total No. of Questions : 6]

SEAT No. :

P4209

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M.E. (Computer)

ADVANCED COMPUTER ARCHITECTURE

(2013 Credit Course) (510103) (Semester - I)

Time : 3Hours] *[Max. Marks : 50*

Instructions to the candidates:

1) ***All Questions are compulsory.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Assume Suitable data if necessary.***

Q1) a) Compare with features different shared memory multiprocessor models. **[5]**

b) State the following terms w.r.t. various interconnect architectures: **[4]**

i) Network diameter

ii) Bisection Bandwidth

iii) Routing function

iv) Multistage Network

OR

a) Draw the dependence graph and analyze the various dependencies among the following statements in a given program. **[5]**

S1 : Load R1, M(100)

S2 : Move R2, R1

S3 : Inc R1

S4 : ADD R2, R1

S5 : Store M(100), R1

b) State and compare Interconnection Networks used in multiprocessor systems. **[4]**

P.T.O.

Q2) a) Define the term Degree of Parallelism (DOP). Describe Average Parallelism in terms of DOP. **[4]**

b) With example, illustrate the mismatch between software and hardware parallelism. How can we match the software and hardware parallelism? **[4]**

OR

a) What is Scalability? Define the term Speedup and Efficiency w.r.t. scalability? How these parameters reflects the performance of parallel computer systems? **[4]**

b) Derive the Amdahl's law for speedup performance. Comment on the major observations and conclusions drawn w.r.t. the speedup obtained. **[4]**

Q3) a) Compare the features and performance of CISC and RISC processor architectures. **[4]**

b) How arithmetic and instruction pipelines are designed? What is the use of Reservation Table? **[4]**

OR

a) State the 4-level memory hierarchy defined for a computer system. How the data transfer takes place between adjacent levels of a memory hierarchy? **[4]**

b) Discuss in brief the different mechanisms implemented in superscalar processor architectures to enhance the performance of Instruction and Arithmetic pipeline. **[4]**

Q4) a) With example state the advantages of vector processing over scalar processing. What is Vectorizing Compiler? State any 2 Vector optimizing functions. **[4]**

b) What is cache coherency? What are the cache write policies used for cache updating? State the 4 states of MESI protocol. **[4]**

OR

a) Discuss and compare between store-and-forward routing and wormhole message routing schemes. **[4]**

b) With example explain the use of Compound Vector Function (CVF) to perform the vector operations. **[4]**

Q5) a) With example explain message passing parallel programming. What is SPMD Programming? **[4]**

b) Explain with example the use of synchronization primitives in parallel programming. **[4]**

OR

a) State and discuss different collective communication functions designed for MPI. **[4]**

b) Explain the support provided by an OS for parallel program execution. Comment on thread and process level parallelism. **[4]**

Q6) a) Explain different services offered by Cloud. What is the difference between public and private cloud? **[5]**

b) Discuss important features of Quantum computing. How these architectures can be used for distributed parallel processing? **[4]**

OR

a) Compare between grid and cloud computing. What is cloud middleware? **[5]**

b) How Neural Networks can be used for distributed parallel computing? Discuss in brief. **[4]**