Total No. of Questions : 6]

SEAT No. :

P2758

[Total No. of Pages : 3

M.E. (Computer) (Semester - I)

ADVANCED COMPUTER ARCHITECTURE

(2013 Pattern)

Time: 3 Hours] *[Max. Marks: 50*

Instructions to the candidates:

1) ***All questions are compulsory.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Assume Suitable data if necessary.***

Q1) a) Draw the dependence graph and analyze the various dependencies among the following satements in a given program **[6]**

S1 : Load R1, M(100)

S2 : Move R2, R1

S3 : Inc R1

S4 : ADD R2, R1

S5 : Store M(100), R1

b) Classify Hazards and state different types of data hazards. **[3]**

OR

a) Discuss in brief the concept of fine grain and coarse grain scheduling. Illustrate with example the node duplication solution w.r.t. static multiprocessor sheduling. **[6]**

b) Distinguish between vector and array processors. State the operational model of SIMD Computer. **[3]**

Q2) a) Define the term Degree of Parallelism (DOP). Describe Average Parallelism in terms of DOP. **[4]**

b) Derive the Amdahl's law for speedup performance. **[4]**

P.T.O.

OR

a) Compare the SIMD architecture with MIMD. Comment on the performance of both w.r.t. parallel processing. **[4]**

b) What is Scalability? Define the term Speedup and Efficiency w.r.t. scalability. **[4]**

Q3) a) Discuss in brief the different mechanisms implemented in superscalar processor architectures to enhance the performance of Instruction and Arithmetic pipeline. **[4]**

b) Compare the features and performance of CISC and RISC processor architectures. **[4]**

OR

a) Explain in brief, a control strategy implemented for job sequencing problem w.r.t. pipelined architecture. **[4]**

b) State and define the parameters associated with the memory technology and storage organization. **[4]**

Q4) a) Discuss the Necessity of cache coherency in multi-processor system. State two commonly used write policies and define 4 states of Pentium MESI protocol. **[4]**

b) With state transition diagram explain write Invalidate Cache coherency protocol. **[4]**

OR

a) What are multi-threaded architectures? Discuss the various performance parameters of multi-threaded processor architectures. **[4]**

b) With example explain the use of Compound Vector Function (CVF) to perform the vector operations. **[4]**

Q5) a) With example explain message passing parallel programming. What is SPMD Programming? **[4]**

b) Compare between MPI and PVM. Discuss the important features of these message passing libraries. **[4]**

OR

a) Discuss with example any Three optimizing/Vectorizing functions designed for optimizing compilers. **[4]**

b) Explain with example the use of synchronization primitives in parallel programming. **[4]**

Q6) a) Discuss important features of Neuro computing. Explain how Neural Networks can be used for distributed parallel computing. **[6]**

b) Compare between grid and cluster computing. **[3]**

OR

a) Explain the following terms w.r.t. Grid computing– **[6]**

i) Middleware ii) OGSA iii) OGSI

b) Discuss important features of Quantum computing. **[3]**