

Total No. of Questions :10]

SEAT No. :

P1811

[4859]-214

[Total No. of Pages :3

B.E. (Computer)

**ADVANCED COMPUTER ARCHITECTURE AND COMPUTING
(2008 Pattern) (Semester - II)**

Time : 3 Hours]

[Max. Marks :100

Instructions to the candidates:

- 1) *Answer any three questions from each section.*
- 2) *Answers to the two sections should be written in separate books.*
- 3) *Neat diagrams must be drawn wherever necessary.*
- 4) *Figures to the right indicate full marks.*
- 5) *Assume suitable data if necessary.*

SECTION - I

Q1) a) Explain following classification approaches for multiprocessor: [12]

- i) Degree of coupling
- ii) Memory access
- iii) Flynn's classification
- iv) Feng's classification

b) List and explain the basic issues in parallel processing. [6]

Q2) a) Consider a dynamic pipelining with five segments S_1, S_2, S_3, S_4 and S_5 characterized by following reservation table [12]

	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
S_1	X								X
S_2		X	X					X	
S_3				X					
S_4					X	X			
S_5							X	X	

P.T.O.

- i) Determine latencies in the forbidden list (F) and the collision vector(C)
 - ii) Draw the state diagram for uniform pipeline
 - iii) Calculate sample cycles and greedy cycles
 - iv) Determine Minimum Average Latency (MAL)
- b) How loop-unrolling technique improves performance of pipelining?[4]

Q3) a) What are characteristics of vector processors? Explain implementation of following loop in conventional scalar processor and vector processor. [8]

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DO 100    I = 1, N
          A(I) = B(I) + C(I)
100      B(I) = 2* A(I+1)

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- b) Explain following pipelined vector processing methods with respect to vector summation computation. [8]
- i) Vertical Processing
 - ii) Vector Looping

How intermediate results are handled in both the cases?

- Q4)** a) Draw and explain two different configurations of array processors. What the network design decisions are for inter PE communication? [8]
- b) Consider a linear array of P processors. N keys have to be sorted parallel. Initially N keys are equally divided among all processors. Assuming SIMD architecture, write a parallel algorithm to sort N keys. [8]

Q5) Write short notes on any two: [16]

- a) Systolic array architecture
- b) Bus arbitration techniques in multiprocessing systems
- c) VLIW processor

SECTION - II

- Q6)** a) List and explain various design issues involved in designing multiprocessor system. [9]
- b) Explain following types of network used to implement processor-memory interconnection with respect to shared memory multiprocessor system. [9]
- i) Multiport Memory
 - ii) Multistage Network
- Q7)** a) Explain following issues in multiprocessor systems [8]
- i) Inter process communication
 - ii) Synchronization software mechanism
- b) What are the different alternatives for interconnecting processors and memory with respect to shared memory multiprocessor systems? [8]
- Q8)** a) What is basic concept of Multithreading? Explain multithreaded architectures and it's computational model for parallel processing systems. [8]
- b) Discuss salient features of parallel processing languages. [8]
- Q9)** a) What are the features of Scalable Processor Architecture? Explain register windows and its parameter passing between procedures of SPARC architecture. [8]
- b) Discuss Cache Coherence Problem and its solutions. [8]
- Q10)** Write short note on any two: [16]
- a) Neuro Computing
 - b) Latency hiding techniques
 - c) Optical computing

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